SC2001 USB-PD Controller with Multiple Fast Charge Protocols Integrated

1 Description

The SC2001 is a highly integrated PD controller. It complies with the latest USB Type-C and PD 3.0 standards and supports the most popular high voltage fast charge protocols with up to 4x DPDM interfaces. The IC targets for notebooks, power banks and other mobile equipment applications.

The SC2001 supports wide operation voltage range with 30V maximum rating, and without the need of an external LDO. It minimizes external components by integrating USB PD baseband PHY, Type-C detection, voltage and current sense, 10-bit DAC for VBUS regulation, 10-bit ADC, shunt regulator, VBUS discharging path, the NMOS gate driver, I2C interface and protection circuits, so to allow easy system design and low BOM cost. Its embedded micro-controller and 32-KB MTP provide highly flexible and cost effective solution to many applications.

The SC2001 supports various protection mechanisms, including over voltage protection, under voltage protection, over current protection, short circuit protection, over temperature protection, DP/DM pin over voltage protection, and CC pin over voltage protection, so to effectively ensure the stable and reliable operation of the system.

The SC2001 is available in 32-pin QFN packages.

2 Features

- **USB Type-C**
  - Support Type-C DRP protocols
  - Configurable resistors R_P and R_D
  - Support Rd when battery is dead
- **USB Power Delivery**
  - Support DFP / UFP / DRP USB PD 3.0
  - Hardware BMC transmitter and receiver
  - Full feature physical layer
  - Hardware CRC
  - Hardware reset
  - Integrate PD 3.0 protocol engine
- **Up to 4x DPDM Fast Charging Interface**
  - Up to 3x hardware controlled DPDM Interface
  - 1x firmware controlled DPDM interface
  - Support Apple charging, BC1.2, DCP, HVDCP, FC, AFC, FCP, and other proprietary charging protocols
- **Power**
  - Wide operation range: 2.7V to 24.5V (30V tolerant)
  - Integrated 5V and 1.8V LDOs
- **MCU Subsystem**
  - Integrated CPU
  - 32-KB MTP and 2-KB Ram
  - Support I2C interface and multiple I/Os
  - CC program function
- **Analog Block**
  - 10-bit DAC for voltage regulation
  - Up to 8-channel 10-bit ADC to monitor the voltage / current / external signals
  - Integrated current sense amplifier
  - Integrated NMOS gate driver for isolation MOS
  - Integrated shunt regulator
  - Integrated VBUS discharging paths at both sides of isolation MOS
- **Protections**
  - On chip OVP, OCP, SCP, UVP and OTP
  - VBUS to CC / DPDM short protection
- **Package**
  - 32-pin QFN

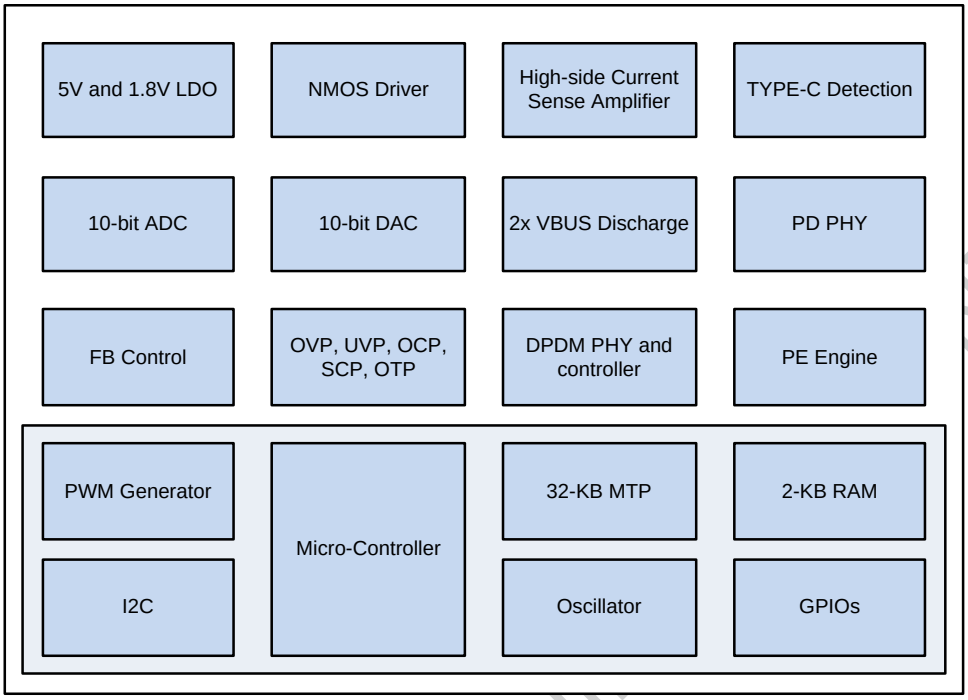
3 Applications

- Power Bank
- Notebook, Tablet
- Other fast charge instruments

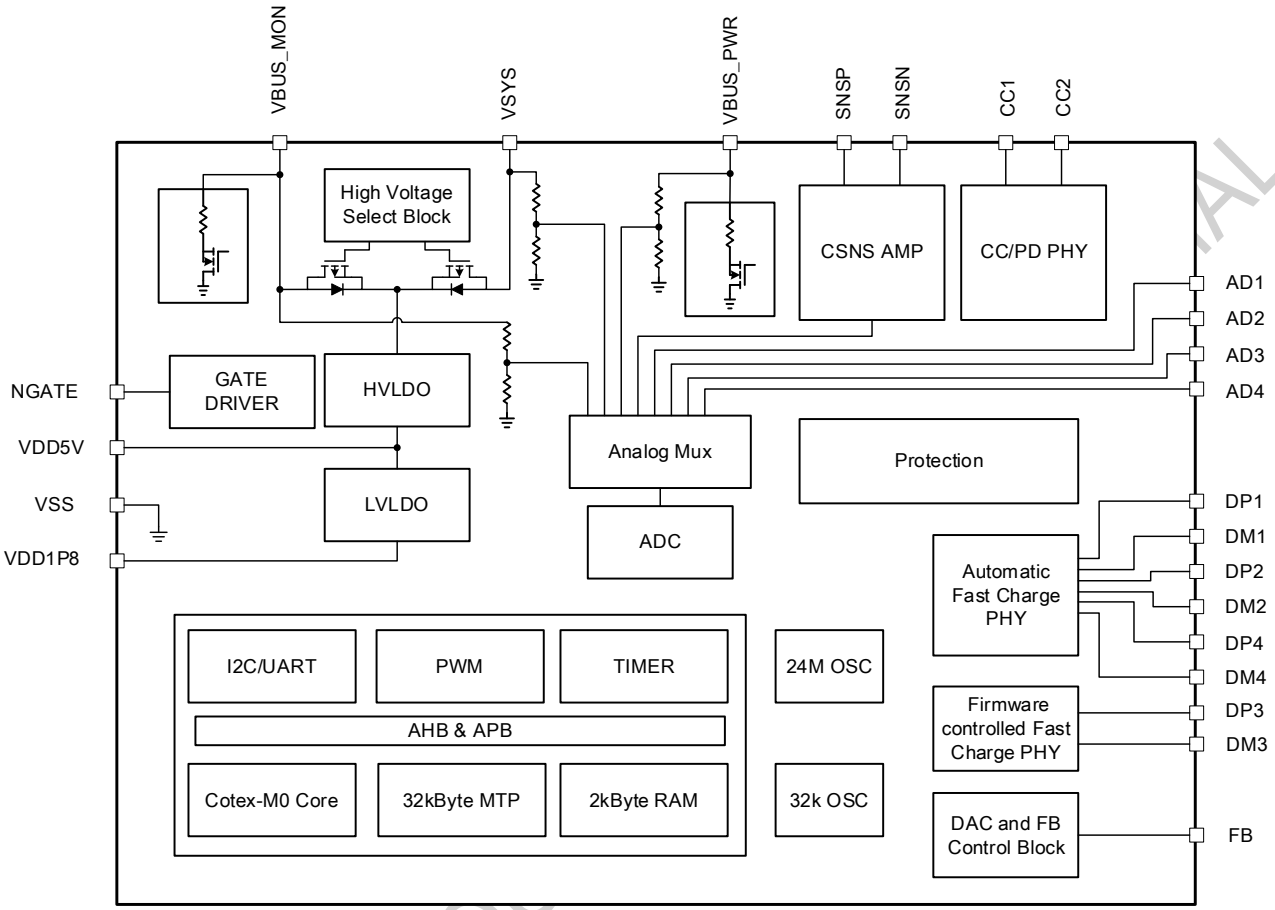
4 Device Information

Part Number	Package	BODY SIZE
SC2001QDER	QFN-32	4mm x 4mm x 0.75mm

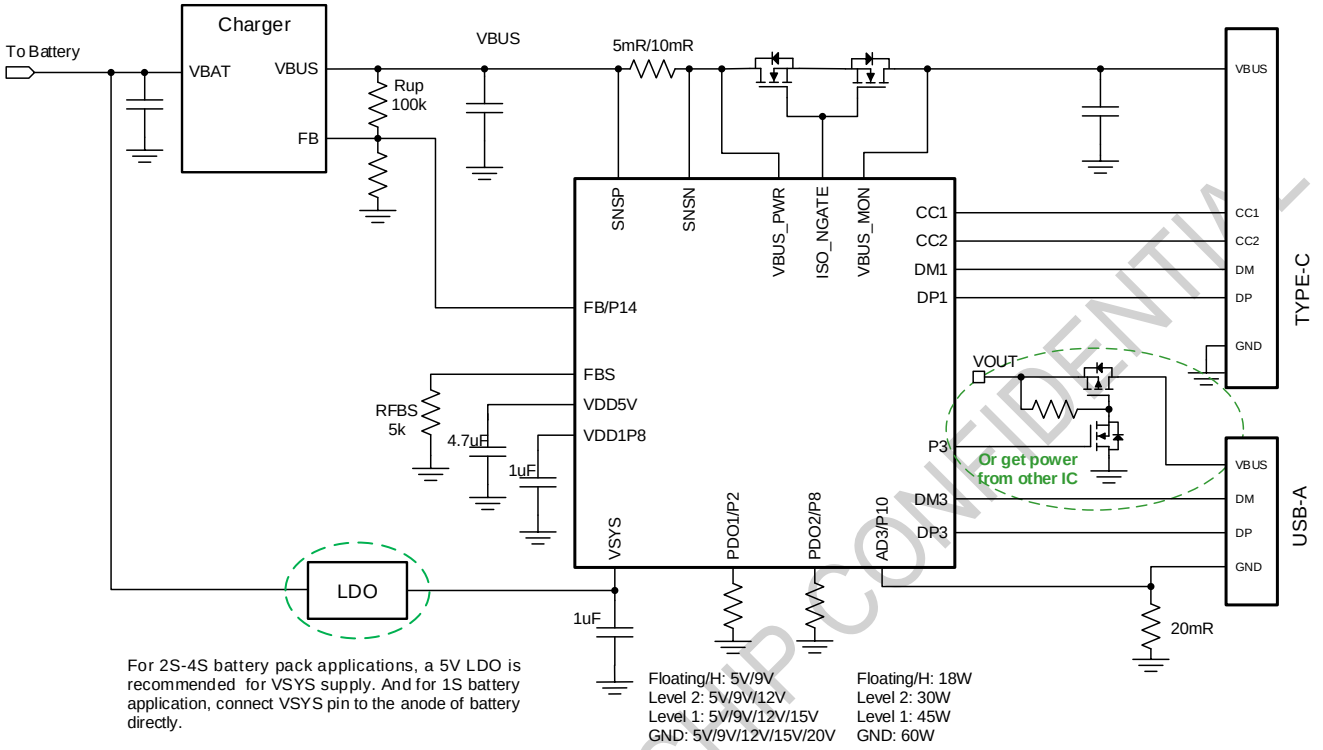
5 Logic Block Diagram



6 Function Block Diagram

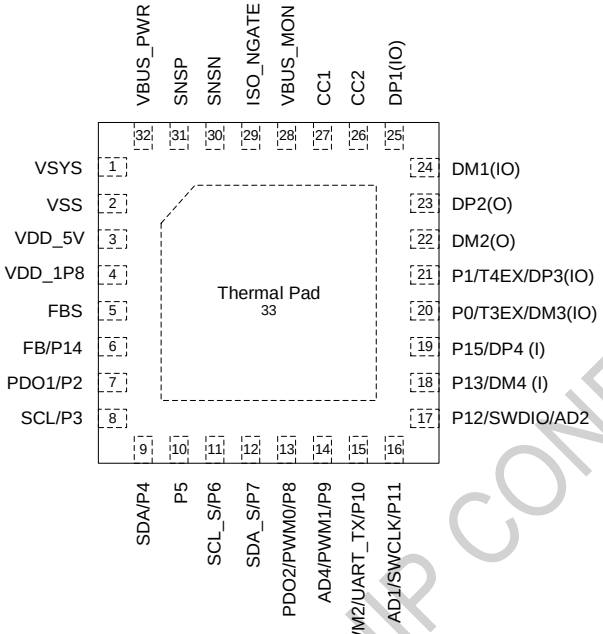


7 Typical Application Diagram



8 Terminal Configuration and Functions

PINOUT of SC2001 (TOP VIEW)



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VSYS	I	The power supply to the IC. Can be connected to the battery.
2	VSS	IO	Ground
3	VDD_5V	O	Output of internal 5V LDO regulator. Supply current to internal circuits. Connect at least 4.7 µF MLCC close to the pin.
4	VDD_1p8	O	Output of internal 1.8V LDO regulator. Supply current to internal digital circuits. Connect at least 1 µF MLCC close to the pin.
5	FBS	I	FBS: used to set the bias current when FB control is used to adjust the output voltage of power IC. Leave this pin floating if FB control is not used.
6	FB	O	If FB control is adopted to adjust the output voltage of the power IC, connect this pin to the feedback divider of the power IC. If FB control is not adopted, leave this pin floating or use this pin as GPIO port P14.
	P14	I/O	General purpose IO
7	PDO1	I	Power data object setting pin 1. Connect a resistor from this pin to ground to set the VBUS voltage.
	P2	I/O	General purpose IO
8	SCL	O	I2C(Master) interface clock.

	P3	I/O	General purpose IO
9	SDA	I/O	I2C(Master) interface data.
	P4	I/O	General purpose IO
10	P5	I/O	General purpose IO
11	SCL_S	I/O	I2C(Slave) interface clock.
	P6	I/O	General purpose IO
12	SDA_S	I/O	I2C(Slave) interface data.
	P7		General purpose IO
13	PDO2	I/O	Power data object setting pin 2. Connect a resistor from this pin to ground to set the VBUS power.
	PWM0	O	PWM0 output
	P8	I/O	General purpose IO
14	AD4	I	A/D Converter input channel 4
	PWM1	O	PWM1 output
	P9	I/O	General purpose IO
15	AD3	I	A/D Converter input channel 3
	PWM2	O	PWM2 output
	UART_TX	O	UART transmitter pin
	P10	I/O	General purpose IO
16	AD1/	I	A/D Converter input channel 1
	SWCLK	I	Serial Wire Debug (SWD) interface clock
	P11	I/O	General purpose IO
17	AD2	I	A/D Converter input channel 2
	SWDIO	I	Serial Wire Debug (SWD) interface data
	P12	I/O	General purpose IO
18	DM4(I)	I/O	DM line of the fast charging interface 4. This port is hardware controlled, and can only be used as charge-in port
	P13	I/O	General purpose IO
19	DP4(I)	I/O	DP line of the fast charging interface 4. This port is hardware controlled, and can only be used as charge-in port
	P15	I/O	General purpose IO
20	DM3	I/O	DM line of the fast charging interface 3. This port is firmware controlled, and can be used as charge-in port and also discharge-out port
	T3EX	I	Input capture pin for timer 3
	P0	I/O	General purpose IO

21	DP3	I/O	DP line of the fast charging interface 3. This port is firmware controlled, and can be used as charge-in port and also discharge-out port
	T4EX	I	Input capture pin for timer 4
	P1	I/O	General purpose IO
22	DM2	O	DM line of the fast charging interface 2. This port is hardware controlled, and can only be used as discharge-out port
23	DP2	O	DP line of the fast charging interface 2. This port is hardware controlled, and can only be used as discharge-out port
24	DM1	I/O	DM line of the fast charging interface 1. This port is hardware controlled, and can be used as charge-in port and also discharge-out port
25	DP1	I/O	DP line of the fast charging interface 1. This port is hardware controlled, and can be used as charge-in port and also discharge-out port
26	CC2	I/O	CC2 line of USB Type-C port
27	CC1	I/O	CC1 line of USB Type-C port
28	VBUS_MON	I	Connected to the VBUS line of the USB Type-C port. It can supply current to the chip, and is also used to sense the VBUS voltage of the port. It is recommended to connect at least 1μF bypass capacitor from this pin to ground close to the IC.
29	ISO_NGATE	O	Gate driver of the external isolation NMOS.
30	SNSN	I	Negative input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
31	SNSP	I	Positive input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
32	VBUS_PWR	I	Connected to VBUS power node of the power IC. It is used to sense the VBUS voltage of the power IC. It is recommended to connect at least 1μF bypass capacitor from this pin to ground close to the IC.
33	Thermal Pad	-	Connect this pad to VSS

9 Specifications

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VBUS_PWR, VBUS_MON, SNSP, SNSN, ISO_NGATE, CC1, CC2, VSYS, FBS	-0.3	30	V
	DP1, DM1, DP2, DM2	-0.3	18	V
	FB, VDD_5V, GPIO, DP3, DM3, DP4, DM4(3)	-0.3	5.5	V
	VDD_1P8	-0.3	1.98	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Connect a resistor (>=10ohm) to DM/DP pin, outside absolute maximum ratings could be upgrade to 12V.

9.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-32 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance		°C/W
θ_{JC}	Junction to case resistance		°C/W

(1) Measured on JESD51-7, 4-layer PCB.

9.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except CC1, CC2, DP1, DM1, DP2, DM2, DP3, DM3, DP4, DM4	-2	2	kV
		DP1, DM1, DP2, DM2(4)	-6	6	kV
		CC1, CC2, DP3, DM3, DP4, DM4	-8	8	kV
	Charged device model (CDM) ESD stress voltage(3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(4) Add series resistor (49Ω) and ESD cell can reach ±8kV ESD performance

9.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VBUS_PWR	VBUS_PWR operation voltage	2.7		24.5	V

VBUS_MON	VBUS_MON operation voltage	2.7		24.5	V
VSYS	VSYS operation voltage	2.6		24.5	V
C_{VBUS_PWR}	Bulk capacitor at VBUS_PWR close to the VBUS node of the power IC	30		200	μF
	Capacitor at VBUS_PWR pin close to the IC		1		μF
C_{VBUS_MON}	Capacitor at VBUS line close to the Type-C port	0.1		10	μF
	Capacitor at VBUS_MON pin close to the IC		1		μF
C_{VDD_5V}	Capacitor at VDD_5V pin	4.7			μF
C_{VDD_1p8}	Capacitor at VDD_1p8 pin		1		μF
R_{SNS}	Current sense resistor between SNSP and SNSN pins	5	10	10	mR
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

9.5 Electrical Characteristics

T_J= 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{VBUS_MON}	VBUS_MON supply range		2.7		24.5	V
V_{SYS}	VSYS supply range		2.7		24.5	V
$V_{BUS\_MON\_UVLO}$	VBUS_MON under voltage lockout threshold				2.85	V
	Hysteresis			200		mV
V_{SYS_UVLO}	VSYS under voltage lockout threshold				2.6	V
	Hysteresis			200		mV
I_Q	Quiescent current during active mode	VSYS=8V, VBUS_MON= floating, all module is active		8		mA
I_{SLP}	Quiescent current during deep sleep mode	Sleep mode is enabled, only CCx block works		80		μA
5V REGULATOR						
V_{DD_5V}	5V LDO regulation voltage	VBUS_MON = 5.5~24.5V, active mode, VSYS = floating	4.85	5	5.15	V
$I_{VDD\_5V\_LIM}$	5V regulator output current limit	VBUS_MON = 8~24.5V, VDD_5V = 4.5V		80		mA
$I_{VDD\_5V\_SCP}$	5V regulator short circuit foldback limit	VBUS_MON = 8~24.5V, VDD_5V = 0V		30		mA
1.8V REGULATOR						
V_{DD_1P8}	1.8V LDO regulation voltage	VDD_5V = 5V, active mode, IOUT = 0~30mA	1.746	1.8	1.854	V
CLOCK						
f_{HF_OSC}	High frequence OSC			24		MHz
f_{LF_OSC}	Low frequence OSC			32		kHz
VBUS MONITOR						
K_V	Ratio from VSYS/ VBUS_PWR/ VBUS_MON to the input of ADC			1/25		
$V_{BUS\_MON\_POR}$	VBUS_MON_POR bit comparator threshold, at VBUS_MON pin	Rising edge	4	4.2	4.4	V
		Falling edge	3.33	3.5	3.67	V
$V_{OVP\_VBUS\_PWR}$	OVP threshold for VBUS_PWR	OVP_SET = 00b, Rising edge	24	25	26	V
		Hysteresis		0.2		V
		OVP_SET = 01b, Rising edge	17.28	18	18.72	V
		Hysteresis		0.2		V
		OVP_SET = 10b, Rising edge	13.44	14	14.56	V
		Hysteresis		0.2		V
$V_{OVP\_VBUS\_MON}$	OVP threshold for VBUS_MON	OVP_SET = 00b, Rising edge	24	25	26	V

		Hysteresis		0.2		V
		OVP_SET = 01b, Rising edge	17.28	18	18.72	V
		Hysteresis		0.2		V
		OVP_SET = 10b, Rising edge	13.44	14	14.56	V
		Hysteresis		0.2		V
$R_{VBUS\_MON\_DCG}$	VBUS_MON discharge equivalent resistance	MON_DCH_CTRL = 00	0.4	0.5	0.6	kΩ
		MON_DCH_CTRL = 01	0.8	1	1.2	kΩ
		MON_DCH_CTRL = 10	1.6	2	2.4	kΩ
		MON_DCH_CTRL = 11	3.2	4	4.8	kΩ
$R_{VBUS\_PWR\_DCG}$	VBUS_MON discharge equivalent resistance	PWR_DCH_CTRL = 00	0.4	0.5	0.6	kΩ
		PWR _DCH_CTRL = 01	0.8	1	1.2	kΩ
		PWR _DCH_CTRL = 10	1.6	2	2.4	kΩ
		PWR _DCH_CTRL = 11	3.2	4	4.8	kΩ
CURRENT SENSE						
K_I	Gain from current sense to ADC/comparators	DIR =0 / DIR=1		15		
V_{SCP}	SCP threshold	Measured as SNSP-SNSN (DIR = 1) and SNSN-SNSP (DIR = 0), SCP_SET = 1, Rising edge	90	100	110	mV
		Hysteresis		1.35		mV
		DIR = 0/1, SCP_SET = 0, Rising edge	45	50	55	mV
		Hysteresis		1.35		mV
V_{OCP}	OCP threshold	Measured as SNSP-SNSN (DIR = 1) and SNSN-SNSP (DIR = 0) OCP_SET = 00b, Rising edge	20.25	22.5	24.75	mV
		Hysteresis		1.35		mV
		DIR = 0/1, OCP_SET = 01b, Rising edge		37.5		mV
		Hysteresis		1.35		mV
		DIR = 0/1, OCP_SET = 10b, Rising edge		45		mV
		Hysteresis		1.35		mV
		DIR = 0/1, OCP_SET = 11b, Rising edge		75		mV
		Hysteresis		1.35		mV
GATE DRIVER						
V_{DRV}	Driving voltage, measured as ISO_NGATE VBUS_PWR (DIR=0)	VDD_5V = 5V			5	V

	or ISO_NGATE-VBUS_MON (DIR=1)					
V_{CLMP_GS}	Driver clamp voltage			10		V
R_{DRV_UP}	Driver pull up resistance	DRV_UP_SET = 00		200		kΩ
		DRV_UP_SET = 01		150		kΩ
		DRV_UP_SET = 10		100		kΩ
		DRV_UP_SET = 11		50		kΩ
R_{DRV_DWN}	Driver pull down resistance	DRV_DWN_SET = 0		2		kΩ
		DRV_DWN_SET = 1		10		kΩ
ADC						
V_{REF}	1.3V reference voltage for ADC			1.3		V
	0.65V reference voltage for ADC			0.65		V
INL	Integral non-linearity		-1.5		2.0	LSB
DNL	Differential non-linearity		-0.5		0.5	LSB
DAC						
t_{slew}	DAC slew rate	Ramp up and ramp down		10		μs/ step
CC LOGIC						
CCX rating	CCx pin voltage rating		25			V
$I_{CC\_80\mu A}$	CC1/2 pull up current	VCC1 = 1.7V to 5.5V CSRC_I = 00	64	80	96	μA
$I_{CC\_180\mu A}$	CC1/2 pull up current	VCC1 = 1.7V to 5.5V CSRC_I = 01	165.6	180	194.4	μA
$I_{CC\_330\mu A}$	CC1/2 pull up current	VCC1 = 1.7V to 5.5V CSRC_I = 10	303.6	330	356.4	μA
R_{PD_CC}	CC1/2 pull down resistor	VCC1 = 0V to 2.5V		5.1		kΩ
R_{CC_OPEN}	CC1/2 open impedance	CC1/2 in disable status or error status CC_ROLE = 11	126			kΩ
$d_{SRC.DRP}$	Percent of time that a DRP shall advertise as source during tDRP		30%	60%	70%	
$V_{TH\_6.15V}$	Comparison threshold at CC1/CC2 pin	CCx OVP detection		6.15		V
DP/DM						
R_{SHORT}	DP DM short resistance			20	40	Ω
R_{DM_DWN}	DP/DM pull down resistance	source/HVDCP, DM		19.53		kΩ
R_{DP_LKG}	DP pin leakage resistance	source/after exit Apple mode, DP		500		kΩ
I2C						

V_{IL}	Input low voltage threshold	SCL, SDA	0.4			V
V_{IH}	Input high voltage threshold	SCL, SDA			1.2	V
$I_{SINK\_SDA\_SCL}$	Sink current	For SCL, SDA VSCL/SDA=0.4V		100		mA
I_{SINK_INT}	Sink current	For INT pin, VINT = 0.4V		4		mA
t_{PULSE}	INT pull low pulse width		0.5	1	1.5	ms
GPIO						
V_{IH_GPIO}	Input voltage high threshold	VDD_5V = 2.7V ~ 5V measured as VIO/VDD_5V			0.7	V
V_{IL_GPIO}	Input voltage low threshold	VDD_5V = 2.7V ~ 5V measured as VIO/VDD_5V	0.3			V
V_{OH_GPIO}	Output voltage high threshold	VDD_5V = 5V apply 4mA sink current from IO pin to GND externally	4.5			V
V_{OL_GPIO}	Output voltage low threshold	VDD_5V = 5V apply 10mA source current from VDD_5V to IO pin externally			0.5	V
V_{PU}	Pull up resistor value at GPIO pin	VDD_5V = 2.7V ~ 5V		5.6		kΩ
V_{PD}	Pull down resistor value at GPIO pin	VDD_5V = 2.7V ~ 5V		5.6		kΩ

10 Detailed Description

10.1 Power Supply

SC2001 provides two power supply input pins VBUS_MON and VSYS. The operation ranges are as follows:

VBUS_MON = 2.7V ~ 24.5V

VSYS = 2.6V ~ 24.5V

VBUS_MON shall be connected to the VBUS line of the USB Type-C port. VSYS is suggested to connect to the battery. At least 1μF bypass capacitor should be connected from the supply pin to the ground close to the IC.

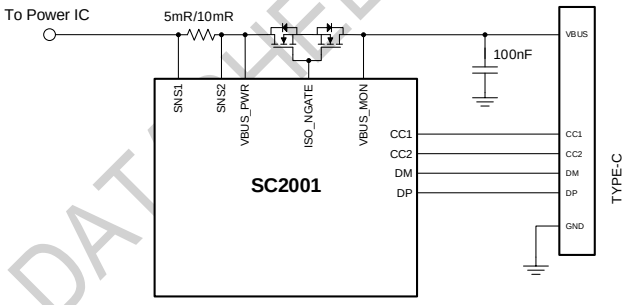
The IC selects the higher voltage of VBUS_MON and VSYS as the input of the internal 5V LDO regulator. Its output VDD_5V powers the internal analog circuit. The VDD_5V can also provide a current up to 10mA to other chips in the system. The VDD_5V also functions as the input of the internal 1.8V LDO regulators, and the output VDD_1P8 is used to power the digital circuit of the IC.

The 5V LDO and 1.8V LDO keeps working in sleep mode, providing at least 10mA current capacity to ensure normal operation of the internal circuit.

10.2 NMOS Gate Driver

The type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. So the SC2001 provides an NMOS gate drive to control the isolation MOSFET between the power IC and the Type-C port.

The gate driver is controlled by register bit. When the driver is turned on, the VGS is equal to VDD_5V. The IC provides 4 different pull-up capabilities from 80kΩ to 300kΩ, and 2 pull-down capabilities at 2kΩ or 15kΩ, so to suit different MOSFETs.



10.3 VBUS Discharging Paths

The IC integrates two VBUS discharging paths (typ. 500Ω resistance) from VBUS_MON and VBUS_PWR pins to ground respectively. The two paths help drain the residual charge on the bulk capacitors so to meet the type-C and USB PD specification timing on a detach condition. The discharging paths are turned on/off through register settings.

10.4 Current Sense Amplifier

SC2001 has a built-in high-precision current amplifier, which is used to amplify the voltage drop between SNSP and SNSN pins, so to monitor the current for the Type-C port.

The current direction is decided by the port role automatically. When the Type-C port functions as a DFP port (power provider), the current from SNSP to SNSN is monitored; if as a UFP port (power consumer), the current from SNSN to SNSP is monitored.

The current sense resistor shall be put at the high side of the port. The input range of the amplifier covers +/-100mV, with a fixed gain of 15. The output of the amplifier is sent directly to the ADC for sampling.

10.5 ADC

In the Type-C, USB PD or other quick charge applications, it is necessary to monitor the VBUS voltage and current. For the devices where battery cells are embedded, the battery voltage needs to be monitored as well. The SC2001 integrates a 10-bit successive approximation Analog to Digital Converter (SAR ADC) with a reference voltage of 0.65V or 1.3V at a sampling rate of 10kHz.

The ADC supports eight-channel input as below. For VBUS_MON, VBUS_PWR and VSYS, an internal ratio of 1/25 is built in.

AD_SRC_SEL[2:0]	Input Signal	Note
000	1/25x VBUS_MON	with 1/25 internal divider
001	1/25x VBUS_PWR	with 1/25 internal divider
010	15x (SNSP – SNSN) or 15x (SNSN – SNSP)	with 15x current sense amplifier
011	1/25 x VSYS	with 1/25 internal divider
100	AD1	
101	AD2	
110	AD3	
111	AD4	

10.6 FB Control through DAC

For power provider application, after the portable device is inserted and the handshake or communication is completed, the adjustment of the output voltage of the power IC is normally needed to satisfy the PDO or fast charge

requirements. A 10-bit Digital to Analog Converters (DAC) is built in to control the FB signal, so to adjust the output voltage of the power IC. The output voltage can be increase or decrease with 20mV/step according to the register setting. This is called the FB control way.

When voltage up is set, the FB pin of the SC2001 sinks a current; when voltage down is set, the FB pin sources a current. A high precision resistor connected from FBS pin to ground is used to set the FB control current reference. The FBS resistor shall be just 1/5 value of the Rup resistor. The Rup is the up resistor of the feedback divider of the power IC, and normally 100kΩ is suggested. The feedback divider and the FBS resistor decide the output voltage accuracy, so high precision resistors with at least ± 1% are required.

When reading DAC registers, the real time value is read; when a target is written to the DAC registers, the SC2001 adjust the DAC value up or down to the target gradually with 10 μs /step. If the target is changed during the process, the DAC will change to the new target from the real time value.

Besides FB control, the SC2001 can also control the output voltage of the power IC through I2C communication if the power IC also supports voltage adjustment through I2C. In this case, the FB pin can be used as a GPIO pin, and FBS shall be short to ground.

10.6.1 Cable Compensation

The SC2001 can be configured to support cable compensation function when FB control is adopted. When this feature is enabled, the chip will automatically increase the output voltage by 120mV (increase the sink current at FB pin by 1.2 μA) when the voltage drop from SNSP to SNSN exceeds 7mV. The output voltage recovers when the SNSP-SNSN voltage drops below 4mV.

10.7 Type-C Port Function

The SC2001 meets the latest Type-C protocol specification (USB Type-C Specification Release 1.3). It can be configured as DFP, DRP or UFP port freely. When configured as DFP or DRP port, it can support different Rp, and broadcast 900mA, 1.5A or 3A current capacity. When configured with UFP or DRP, it can detect the Rp of CC1 or CC2 so to detect the source current capability. After configuration, the IC runs the state machine automatically and reports the status through registers.

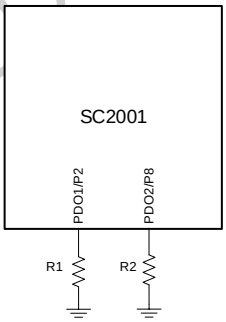
The SC2001 can also support dead battery charging, that is, it applies 5.1kΩ resistor at CC1 and CC2 respectively when the IC is in power down status.

10.8 USB PD Protocol

The SC2001 provides USB PD physical layer for PD protocol communication. It can automatically select either CC1 or CC2 channels to send and receive PD packets according to the insertion direction of type-c port. The firmware controls the PD packets.

10.8.1 PDO Setting

Users can set the PDO voltage, current and power configuration of PD protocol conveniently through PDO pin as below illustrates. The IC detects the PDO pin setting during power on, and updates the setting to firmware through registers. Firmware then controls the PD-phy according to the setting information.



PDO1 Setting				
R1/kOhm	R<95	101<R<360	400<R<660	R>740
Support voltage/V	5/9/12/15/20	5/9/12/15	5/9/12	5/9

PDO2 Setting				
R2/kOhm	R<95	101<R<360	400<R<660	R>740
Support Power/W	60	45	30	18

10.9 DPDM Interface

The SC2001 has four built-in DPDM interfaces, DPDM1-DPDM4. DPDM1 and DPDM3 can be configured as charging in port (consumer) or discharging out port (provider); DPDM2 as discharging out port, and DPDM4 as charging in port. Typically, DPDM1 or DPDM3 can be used to connect to the USB Type-C port. DPDM1, DPDM2 and DPDM3 can be connected to USB-A port, DPDM1, DPDM3, and DPDM4 can be connected to Micro-B port.

Table 1 DPDM Port Configuration

Interface	Charging-in Port (Consumer)	Discharging-out Port (Provider)	Can be configured as			Apple 2.4A	BC1.2 DCP	HVDCP	FC2.0/3.0	Other HV fast charge protocols	Note
			USB-A	Micro-B	TYPE-C						

DPDM1	✓	✓	✓	✓	DFP, DRP, UFP	✓ IN/OUT	✓ IN/OUT	✓ IN/OUT	✓ IN/OUT	✓ OUT	
DPDM2		✓	✓		DFP	✓ OUT	✓ OUT	✓ OUT	✓ OUT	✓ OUT	
DPDM3	✓	✓	✓	✓	DFP, DRP, UFP	✓ IN/OUT	✓ IN/OUT	✓ IN/OUT	✓ IN/OUT	✓ IN/OUT	Firmware Controlled
DPDM4	✓			✓	UFP	✓ IN	✓ IN	✓ IN	✓ IN		

When as discharging-out port, it can support Apple-2.4A, BC1.2 DCP, HVDCP and other mainstream fast charging protocols. When as charging-in port, it supports the detection of APPLE, Samsung, BC1.2, HVDCP and other mainstream fast charging protocols in the market.

10.10 Protections

10.10.1 Over Voltage Protection

The SC2001 monitors the VBUS_PWR and VBUS_MON voltage in real time. Once either voltage exceeds the OVP threshold, the OVP flag is set and the IC forces the NGATE driver off automatically. When the fault is removed, the NGATE driver recovers to normal operation.

The OVP thresholds and the detection deglitch time can be configured through registers.

10.10.2 Under Voltage Protection

The SC2001 also supports the under voltage protection for VBUS_PWR and VBUS_MON.

When the Type-C port functions as a DFP port (power provider), the under voltage protection is triggered when VBUS_PWR is below typ. 2.7V; when as a UFP port (power consumer), the UVP is triggered when VBUS_MON is below typ. 2.7V.

When UVP happens, the UVP flag is set and the IC forces the NGATE driver off. When the fault is removed, the NGATE driver recovers to normal operation.

10.10.3 Over Current Protection

The SC2001 monitors the current of the Type-C port and sets an over-current flag through register when over-current fault is detected. The over-current thresholds corresponding to the voltage drop between SNSP and SNS pins can be set to four levels, which are 22.5mv, 37.5mv, 45mV and 75mV respectively.

The over-current detection deglitch time can be configured to 10ms or 30ms through register bit.

10.10.4 Short Circuit Protection

Besides the over current flag, the SC2001 offers two short-circuit protection thresholds: 50mV and 100 mV respectively. The short circuit detection deglitch time can also be set to 64 µs or 128 µs. Once the short-circuit fault is detected, the SC2001 sets the SCP flag, and forces the NGATE driver off automatically. After the SCP, the NGATE driver can only be reset to normal operation through register manually.

During the isolation MOSFET is turned on, there might be high current to charge the bulk capacitors on VBUS power node or the capacitors of the portable device. In order to avoid the false-trigger of the short circuit protection, user can configure the SC2001 to blank the short circuit protection during NMOS gate driver is on.

10.10.5 Over Voltage Protection for CC and DPDM

The IC supports multiple protection of the interface pin. Once it detects any of the CCx/ DPx/ DMx voltage exceeds 6.2V, the IC will report the over-voltage status.

10.11 MCU Controller

10.11.1 Clock

The SC2001 integrates a 24MHz high frequency clock and a 32kHz low frequency clock. Under normal working condition, high frequency clock and low frequency clock work simultaneously. When in sleep mode, only the 32kHz clock works to reduce the power consumption.

10.11.2 Modes

The SC2001 supports two operating modes: active mode and sleep mode. Under active mode, each function module operates normally. When in sleep mode, only the 32kHz low frequency clock, LDOs, CC1/CC2 interface, and GPIO (I2C Slave interface) work, all other functions are turned off. The quiescent current can be as low as 50 µA in sleep mode.

To enter sleep mode, the current sense function shall be turned manually and then write the Sleep mode control bit.

After entering sleep mode, the system can be awakened by interruptions, including GPIO interrupts, I2C Slave interrupts,

CC interrupts, Watchdog interrupts, and the timer interrupts of the 32kHz clock source.

10.11.3 GPIO

GPIO has input/output direction settings, internal pull-up/pull-down resistor settings, and interrupt edge settings. Please see register map for details.

10.11.4 Interrupts

The IC supports various interrupts, including Timer0 / Timer1/ Timer2 / Timer3 / Timer4 interrupts, PWM0 / PWM1 / PWM2 interrupts, CC/ PD interrupts, ADC interrupt, I2C master/salve interrupts, DPDM1 /DPDM3 interrupts, analog interrupts, WDT interrupt, GPIO0 ~ GPIO8 / GPIO10 / GPIO14 interrupts.

10.11.5 Timers

The SC2001 has five timers, from Timer0 ~ Timer4.

10.11.6 UART

UART can support Tx function but no Rx function.

10.11.7 I2C

The SC2001 has one I2C master interface (I2C_M) and one slave interface (I2C_S). The I2C slave address is (0xE2/0xE3).

10.11.8 Watchdog

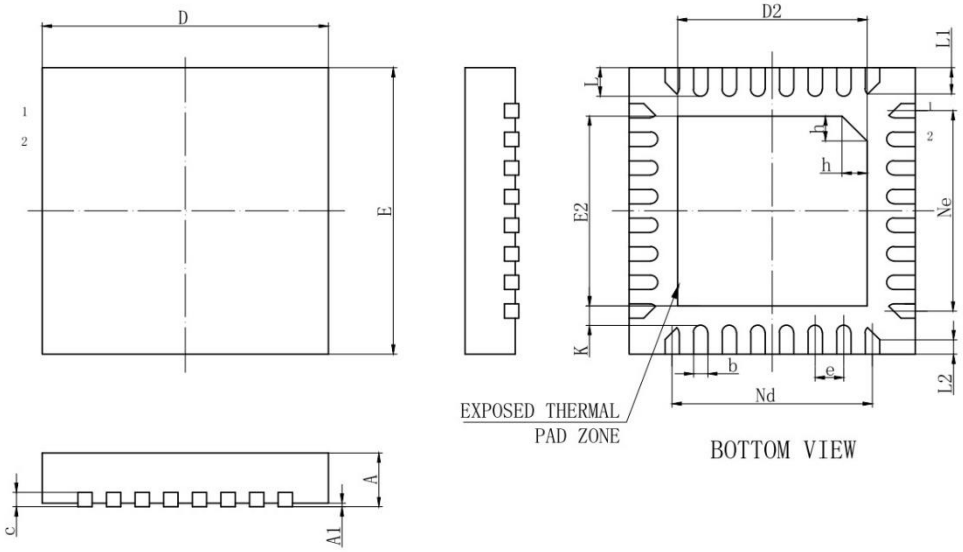
The watchdog is a 32bit counter with 32kHz clock source. When the watchdog is enabled, the watchdog counter starts with the value of register WDT_CNT and counts down. The control register WDT_CTRL can be used to select whether an interrupt or reset signal, or both occurs when the counter overflows (counting to 0).

10.11.9 Programming

The SC2001 provides two independent programming methods, one through I2C_S function, the other through CC1/CC2 pins.

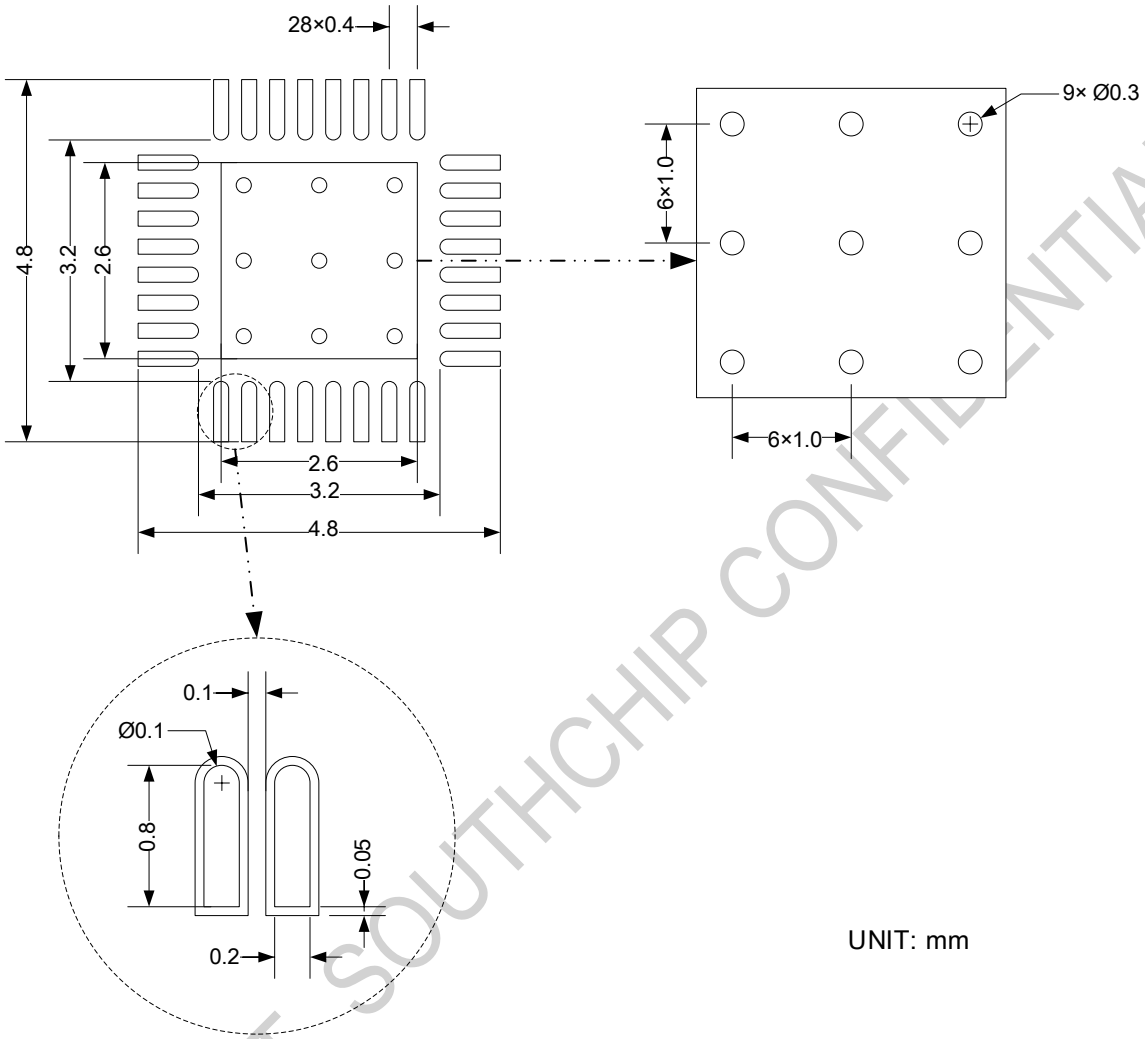
PACKAGE

QFN-32 0404 x 0.75



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	⚠
	0.85	0.90	0.95	⚠
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
c	0.18	0.20	0.25	
D	3.90	4.00	4.10	
D2	2.60	2.65	2.70	
e	0.40BSC			
Nd	2.80BSC			
E	3.90	4.00	4.10	
E2	2.60	2.65	2.70	
Ne	2.80BSC			
K	0.20	-	-	
L	0.35	0.40	0.45	
L1	0.30	0.35	0.40	
L2	0.15	0.20	0.25	⚠
h	0.30	0.35	0.40	
L/F载体尺寸 (MIL)	112*112			

Board Layout Example



UNIT: mm